AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions of claims in the application:

Listing of Claims:

1. (Currently amended) A system that facilitates measurement and correction of overlay between multiple layers of a wafer, comprising:

an overlay target that represents overlay between three or more layers of a wafer; and

a measurement component that determines overlay error existent in the overlay target, and ~~thereby~~ determines overlay error between the three or more layers of the ~~wafer.~~ wafer, where the measurement component comprises a comparison component that compares a captured signature with one or more stored signatures to facilitate determination of overlay error existent in the overlay target.

2. (Original) The system of claim 1, further comprising a control component that utilizes the overlay error determined by the measurement component to correct overlay error between the three or more layers of the wafer.

3. (Currently amended) The system of claim 2, ~~wherein~~ the control component provides more correction in a first dimension and less correction in a second dimension in an instance ~~that precision of overlay alignment is more important~~ in which design rule requirements tolerate less overlay error in the first dimension when compared to the second dimension.

4. (Currently amended) The system of claim 2, ~~wherein~~ a substantial overlay correction between non-adjacent layers of the wafer in a first dimension correlates to a substantial overlay correction between adjacent layers of the wafer in a second dimension.

5. (Currently amended) The system of claim 2, ~~wherein~~ an insubstantial overlay correction between non-adjacent layers of the wafer in a first dimension correlates to an insubstantial overlay correction between adjacent layers of the wafer in a second dimension.

6. (Currently amended) The system of claim 2, ~~wherein~~ the control component manipulates at least one of temperature(s) associated with a process step, pressure(s) associated with a process step, concentration of gas(es) within a process step, concentration of chemical(s) within a process step, composition of gas(es) within a process step, composition of chemical(s) within a process step, flow rate of gas(es) within a process step, flow rate of chemical(s) within a process step, timing parameters associated with a process step, and excitation of voltages associated with a process step.

7. (Currently amended) The system of claim 2, ~~wherein~~ at least one of concentration, rate of flow, and degree of abrasiveness is controlled to correct overlay error.

8. (Currently amended) The system of claim 2, ~~wherein~~ the control component facilitates correction of rotational overlay error.

9. (Currently amended) The system of claim 2, ~~wherein~~ the measurement component and the control component are integrated with at least one process step to facilitate *in situ* correction of overlay error.

10. (Original) The system of claim 2, the control component facilitating simultaneous overlay correction of two or more wafers.

11. (Currently amended) The system of claim 1, ~~wherein~~ the overlay target has a structure of at least one of box-in-box, frame-in-frame, segmented frame, and periodic structure.

12. (Currently amended) The system of claim 1, ~~wherein~~ the overlay target comprises one or more gratings.

13. (Currently amended) The system of claim 1, the measurement component comprising:
an optical microscope utilized to capture an image of the overlay target; and

a comparison component that compares the captured image with one or more stored images, wherein the comparison facilitates determination of overlay error existent in the overlay target.

14. (Currently amended) The system of claim 1, the measurement component further comprising:

a light emitting component that delivers light incident to the overlay target; and

a light capturing component utilized to capture a signature that results from the incident light contacting the overlay target. ~~target; and~~

~~a comparison component that compares the captured signature with one or more stored signatures, wherein the comparison facilitates determination of overlay error existent in the overlay target.~~

15. (Currently amended) The system of claim 1, ~~wherein~~ optical microscopy techniques are utilized to facilitate measurement of overlay error existent in the overlay target.

16. (Currently amended) The system of claim 1, ~~wherein~~ scatterometry techniques are utilized to facilitate measurement of overlay error existent in the overlay target.

17. (Currently amended) The system of claim 1, ~~wherein~~ scanning electron microscopy techniques are utilized to facilitate measurement of overlay error existent in the overlay target.

18. (Currently amended) The system of claim 1, ~~wherein~~ Fourier transform infrared scatterometry techniques are utilized to facilitate measurement of overlay error existent in the overlay target.

19. (Original) A stand-alone metrology unit comprising the system of claim 1.

20. (Original) The system of claim 1, the overlay target associated with a particular die on the wafer.

21. (Original) The system of claim 1, the wafer subdivided into a grid comprising a plurality of cells, wherein the grid facilitates measurement and recordation of overlay error at particular portions of the wafer.

22. (Currently amended) The system of claim [[19]] 21, the wafer discarded if a threshold percentage of cells exhibit a threshold level of overlay error.

23. (Currently amended) A method for measuring and correcting overlay error in more than two layers of a wafer, the method comprising:

generating a multi-layered overlay target, wherein disparate layers of the overlay target represent disparate layers of the wafer; [[and]]

delivering light incident to the overlay target;

capturing a signature that results from the incident light contacting the overlay target; and

comparing the captured signature with one or more stored signatures to facilitate determination of overlay error existent in the overlay target.

~~approximating overlay error of non-adjacent layers of the wafer *via* measuring overlay error between the representative layers of the overlay target.~~

24. (Currently amended) A stand-alone metrology unit utilizing the method of claim [[21]] 23.

25. (Currently amended) The method of claim [[21]] 23, further comprising:

correcting overlay error between non-adjacent layers of the wafer based at least in part on the measured overlay error existent in representative layers of the overlay target.

26. (Currently amended) The method of claim [[23]] 25, the overlay error corrected *via* modifying one or more of temperature(s) associated with a process step, pressure(s) associated with a process step, concentration of gas(es) within a process step, concentration of chemical(s) within a process step, composition of gas(es) within a process step, composition of chemical(s) within a process step, flow rate of gas(es) within a process step, flow rate of chemical(s) within a

process step, timing parameters associated with a process step, and excitation of voltages associated with a process step.

27. (Currently amended) The method of claim [[21]] 23, further comprising approximating overlay error between adjacent layers on a wafer *via* measuring overlay error between the representative layers of the overlay target.

28. (Currently amended) The method of claim [[25]] 27, further comprising correcting overlay error between adjacent layers of a wafer based at least in part on the measured overlay error existent in representative layers of the overlay target.

29. (Currently amended) The method of claim [[26]] 28 further comprising:

substantially correcting overlay error between non-adjacent layers of the wafer in a first dimension; and

substantially correcting overlay error between adjacent layers of the wafer in a second dimension.

30. (Currently amended) The method of claim [[26]] 28, further comprising:

insubstantially correcting overlay error between non-adjacent layers of the wafer in a first dimension; and

insubstantially correcting overlay error between adjacent layers of the wafer in a second dimension.

31. (Currently amended) The method of claim [[26]] 28, further comprising providing a greater amount of overlay correction in one particular direction in comparison to a substantially perpendicular dimension.

32. (Currently amended) The method of claim [[23]] 25, further comprising simultaneously correcting overlay in two or more wafers based at least in part upon the measured overlay error.

33. (Currently amended) A system that corrects overlay error between three or more layers of a wafer, comprising:

means for creating an overlay target, the overlay target representing three or more layers of a wafer;

means for delivering light incident to the overlay target;

means for capturing a signature that results from the light incident to the overlay target;

means for comparing the captured signature with one or more stored signatures to determine overlay error in the overlay target; and

~~means for measuring overlay error on the overlay target, the measurements representing overlay error existent between non-adjacent layers of the wafer; and~~

means for correcting overlay error between non-adjacent layers of the wafer based at least in part on the measurements relating to the overlay target.

34. (Currently amended) A system for correcting overlay error between three or more layers of a wafer, where the system comprises: ~~comprising:~~

a measurement component that comprises:

a light emitting component that delivers light incident to the overlay target;

a light capturing component utilized to capture a signature that results from the incident light contacting the overlay target; and

a comparison component that compares a captured signature with one or more stored signatures to determine overlay error associated with the overlay target; and

a receiving component that receives measurements associated with overlay error between three or more layers of the wafer; and

a control component that effectuates a particular overlay error correction in a first dimension between adjacent layers of the wafer corresponding to a substantially similar overlay error correction in a second dimension between non-adjacent layers of the wafer.